ANSEN An International Manufacturing Company GROUP
ANSEN Corporation

U DFM Checklist

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Design & Component Selection
- ” Each component is or will be readily available in production quantities
- ” Minimize number & number of different components
- ” No components at end-of-life designed in
- ” No sole-source devices, if possible
- ” Multiple manufacturers specified for all components
- ” Second sources checked for mechanical & electrical fit
- ” Component tolerance issues analyzed
- ” Component temperature ranges considered
- ” Use a BGA instead of that huge fine-pitch QFP?
- ” Eliminate trim pots
- ” Design for Environment: for recycle, re-use & repair

General Layout Issues
- ” Visible orientation marks for all polarized components on silkscreen layer
- ” Polarized components (e.g. caps) same direction
- ” Layer #’s visible on pcb or breakoffs, names on artwork

Manufacturing Process for Board Assembly
- ” Workmanship requirements established, e.g. IPC
- ” Number of processes minimized
- ” Hand soldering minimized
- ” Hand insertion and assembly minimized

Through-Hole Components
- ” Unplated tooling holes for through-hole automation
- ” Drill sizes: lead diameter + 0.015" for auto-inserted through-hole DIP, axial and radial components (note some exceptions on unplated single-sided boards)
- ” DIP socket drill holes should be 0.040"
- ” Auto-inserted components on 0E, 90E, 180E or 270E
- ” DIPs oriented same way on volume boards
- ” Axials oriented same way on volume boards
- ” TO-92 layouts are in-line spaced 0.100" pad-to-pad
- ” No stand-up axial components
- ” Minimum 0.010" annular rings on through-hole pads

SMT Land Patterns
- ” Fine-pitch land patterns at 60% pad width/pitch
- ” Land patterns match to actual physical components
- ” Use of land patterns optimized for manufacture
- ” No natural bridges on fine-pitch SMT
- ” Non-solder mask defined (NSMD) pads for BGAs

Wave-Soldered Bottom Side SMT Components
- ” Do you *really* have to do this lower-yielding process?
- ” Bottom-side SMT wave land patterns optimized
- ” Component orientation optimized on waved SMT components, e.g. SOICs, SOT-23s & DPAKs
- ” No wave soldered 4-sided SMT or fine-pitch SMT
- ” Minimum component-to-component spacing is height of tallest of two components.
- ” Other wave solder shadowing considerations
- ” On mixed technology pcbs, no SMT components on bottom within DIP clinch head footprint

Hardware
- ” Stainless-steel on PCB to prevent rusting, repel solder
- ” Tinned PEMs, etc, will solder to board
- ” Phillips or allen head screws for ease of assembly
- ” Silpad washers on power devices where required
- ” Rivscrews possible?
- ” Mounting holes unplated with no pads if possible

Board Mechanicals
- ” 3 fiducial marks 0.060" on each side with SMT
- ” Via holes covered with soldermask - normal strategy except for some ICT enabled designs
- ” Layer stack-up identification on board or breakoff tab
- ” Component to board-edge clearance considerations
- ” Panelization or breakoffs discussed with ANSEN

PC Board Specifications
- ” Optimum board finish specified (e.g. gold flash for boards with FBGA or QFPs 0.020" pitch and smaller)
- ” Boards specified for Bare-Board Test (BBT)
- ” Gerber files generated in RS-274-X format (with embedded aperture lists)
- ” No soldermask between fine-pitch 0.020" or smaller
- ” Controlled impedance specified where required
- ” Any special board materials or construction specified for high-frequency boards.
- ” Liquid photo-imageable soldermask is standard
- ” SMT paste layer(s) with no fiducial or other pads

Test Strategy
- ” Test plan established before design started
- ” Failure modes considered
- ” Choose among self-test, manual functional test, all-boundary-scan board test, automated functional test and in-circuit/combinational test (ICT)
- ” Avoid test turrets & hooks, use SMT loops, if required

In-Circuit Test Mini-Checklist
- ” Schematic review by ANSEN test engineers prior to board layout.
- ” Enables for ICs & oscillators with resistor pull-downs
- ” Unused IC pins for complex ICs have test pads
- ” Boundary scan enabled devices (note they have special chaining and layout requirements)
- ” One test pad per net, accessible from the bottom
- ” More pads for power nets: 0.5A per test point
- ” Minimum test pad is 0.030", prefer 0.040" square
- ” Through-hole leads used as test points - OK
- ” 2 tooling holes required: diagonally opposite, minimum 0.093", 0.125" preferred - UNPLATED
- ” Use of 0.050" & 0.075" center-center test points minimized or eliminated, 0.100" spacing preferred
- ” Pads with via holes used as test points have no soldermask over them, other vias masked
- ” ICT tooling hole to test pad clearance 0.125"
- ” Board edge to test pad clearance 0.100"
- ” On-board batteries have disconnect jumper