

Design and Component Selection

- Each component is or will be readily available in production quantities
- Minimize number & number of different components
- No components at end-of-life designed in
- No sole-source devices, if possible
- Multiple manufacturers specified for components
- Second sources checked for mechanical & electrical fit
- Component tolerance issues analyzed
- Component temperature ranges considered
- Use a BGA instead of that huge fine-pitch QFP
- Eliminate trim pots
- Design for Environment: recycle, re-use & repair

General Layout Considerations

- Visible orientation marks for all polarized components on silkscreen layer
- Polarized components (e.g. caps) same direction
- Manufacturing Process for Board Assembly
- Workmanship requirements established, e.g. IPC
- Number of processes minimized
- Hand soldering minimized
- Hand insertion and assembly minimized

Through-Hole Components

- Unplated tooling holes for through-hole automation
- Drill sizes: lead diameter +0.015"
- DIP socket drill holes should be 0.040"
- Components at 0, 90, 180 or 270 degrees
- Component layout optimized for auto insertion
- DIPs oriented same way on volume boards.
- Axials oriented same way on volume boards
- TO-92 layouts are in-line spaced 0.100" pad-to-pad
- No stand-up axial components.
- Minimum 0.010" annular rings on through-hole pads

SMT Land Patterns

- Fine-pitch land patterns at 60% pad width/pitch
- Land patterns match to actual physical components
- Use of Land patterns optimized for manufacture
- No natural bridges on fine-pitch SMT
- Non-solder mask defined (NSMD) pads for BGAs

Wave-Soldered Bottom-Side SMT Components

- Do you *really* have to do this lower-yielding process?
- SMT wave land patterns optimized
- Component orientation optimized for wave
- No 4-sided SMT or fine-pitch SMT components
- Minimum component-to-component spacing is height of tallest of two components
- Other waver solder shadowing considerations
- On mixed technology PCBs, no SMT components on bottom within DIP clinch head footprint.

Hardware

- Stainless-steel when PCB contact is made
- Favor Torx drive screws for ease of assembly
- Minimize the number of different screw sizes and styles; go for commonality wherever possible
- Torque values are specified for screws and nuts
- Silpad washers on power devices where required
- Mounting holes unplated with no pads if possible

Board Mechanicals

- 3 fiducial marks 0.060" on each side with SMT
- Via holes covered with soldermask-normal strategy except for some ICT enabled designs
- Layer stack-up identification on board or breakaway
- Component to board-edge clearance considerations
- Panelization or breakouts discussed with Ansen

Board Specifications

- Optimal board finish specified (e.g. ENIG for boards with μ BGA or QFPs 0.020" pitch and smaller)
- Boards specified for Bare-Board Test (BBT)
- Gerber files generated in RS-274-X format
- No Soldermasks between fine-pitch 0.020" or smaller
- Controlled impedance specified where required
- Any special board materials or construction specified for high-frequency boards
- SMT Paste layer(s) with no fiducial or other parts
- Ensure post-breakout PCB dimensions and dimensional tolerances are accounted for in the panel design

Test Strategy

- Test plan established before design started
- Failure modes considered
- Choose among self-test, manual functional test, all-boundary- scan board test, automated functional test and in-circuit/combination test (ICT)
- Avoid test turrets & hooks; use SMT loops where on-board test pads are not feasible

In-circuit Test Mini-Checklist

- Schematic review by ANSEN test engineers prior to board layout
- Enables for ICs & oscillators with resistor pull-downs
- Unused IC pins for complex ICs have test pads
- Proper circuit layout for boundary scan devices
- One test pad per net, accessible from the bottom
- More pads for power nets: 0.5A per test point
- Minimum test pad is 0.030", prefer 0.040" square
- Through-hole leads used as test points-OK
- 2 tooling holes required: diagonally opposite, minimum 0.093", 0.125" preferred – UNPLATED
- Use of 0.050" & 0.075" center – center test points minimized or eliminated; 0.100" spacing referred.
- Pads with via holes used as test points have no soldermask over them, other vias masked.
- ICT tooling hole-to-test pad clearance: 0.125"
- Board edge to test pad clearance: 0.100"
- On-board batteries have disconnect jumper